

**SILICON PROCESSING
FOR
THE VLSI ERA**

**VOLUME 2:
PROCESS INTEGRATION**

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2.10.2 Wafer Bonding

A planar process similar to the conventional DI process can be implemented with wafer bonding. In this method, two oxidized silicon wafers are fused together through a high-temperature furnace step. The following approaches have been developed to consummate the bonding:

- Two oxidized-silicon wafers are pressed together and subjected to an oxidizing ambient at 700°C.⁸¹ Bonding under these conditions is believed to occur as a result of the conversion of the gaseous oxygen between the wafers to SiO₂. This conversion is thought to create a partial vacuum that forces the wafers into intimate contact, bringing about the bonding chemical reaction. (This is believed to be a polymerization of silanol bonds to form a siloxane network).
- When a moderate voltage is applied between two silicon wafers, bonding is induced at temperatures of 1100-1200°C (Fig. 2-52).⁸² One advantage of electrostatic bonding is that since no mechanical force needs to be applied to press the wafers together initially, it does not introduce crystal defects into the silicon.
- One oxidized silicon wafer and one bare silicon wafer are cleaned with an H₂O₂-H₂SO₄ mixture. Treatment with an acid solution is then used to form an O-H group on the wafer surfaces. After drying, the wafers are placed face-to-face at room temperature in clean air. A self-adhesive contact is formed, and thereafter no weight or pressure need be applied to the contacted wafers. The bonding is then carried out by a heat treatment of 1100°C in a nitrogen ambient for four hours.⁸³

The SOI structure is also formed in a number of different ways. With one method, a lightly doped epitaxial layer is grown on a heavily doped substrate, and this layer is then thermally oxidized (i.e., to a thickness of 1-2 μm). Following bonding, a preferential etch is used to remove the heavily doped substrate, leaving a thin, lightly doped epitaxial layer above the thermally grown oxide.⁸¹ The active-device layer is

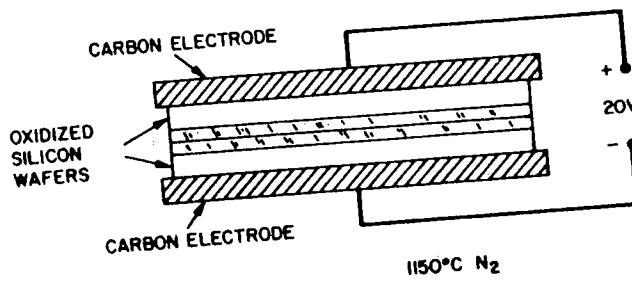


Fig. 2-52 Electrostatic technique for bonding silicon wafers.⁸² Reprinted by permission of the publisher, The Electrochemical Society, Inc.

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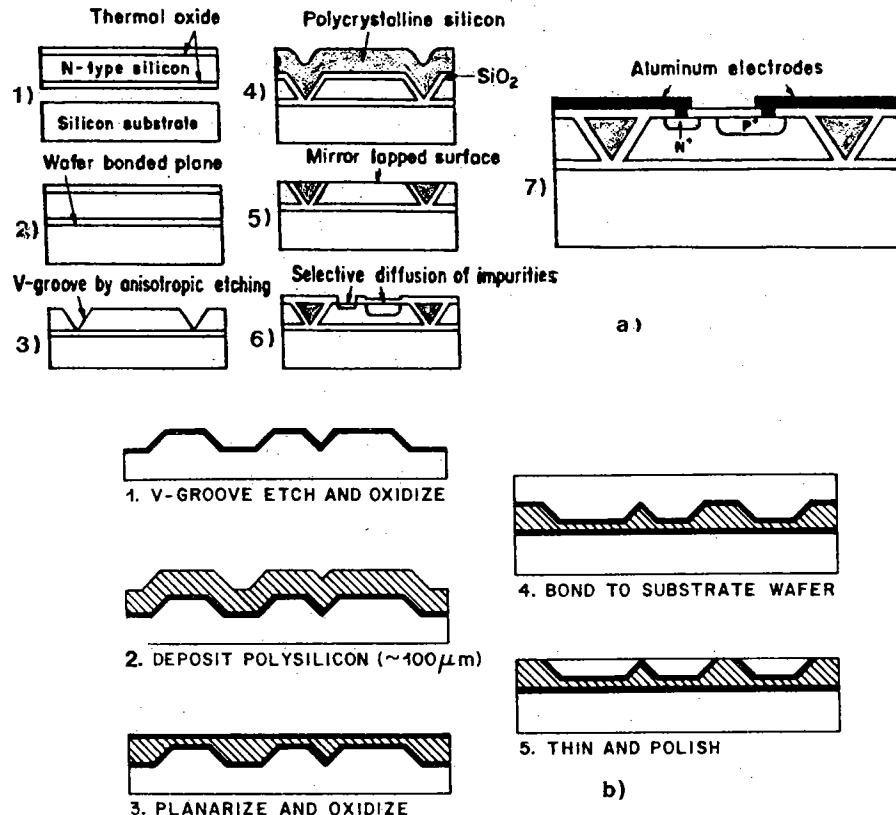


Fig. 2-53 Isolation structure formation in bonded silicon wafers. (a) SDB technique,⁸³ (© 1986 IEEE). (b) Electrostatically bonded technique.⁸² Reprinted by permission of the publisher, The Electrochemical Society, Inc.

determined by the thickness of the epitaxial layer. Alternatively, the heavily doped substrate is removed by lapping, and the remaining epi layer is polished to the desired thickness.⁸⁴

In a second method, the surface of the bonded silicon wafer is V-groove etched and oxidized. A polysilicon film, much thinner than that used in conventional DI, is then deposited, planarized, and oxidized (Fig. 2-53a).⁸³ This wafer is then bonded to another wafer. Finally, the single-crystal silicon of the wafer with the deposited polysilicon is thinned and polished to form dielectrically-isolated active regions.

In yet another approach, the upper part of one of the wafers is chemically polished until a $70\text{-}\mu\text{m}$ -thick Si layer remains (Fig. 2-53b). V-grooves are formed, and SiO_2 is regrown over the surface. Polysilicon is deposited to a thickness of $100 \mu\text{m}$ and the wafer is again polished until most of the polysilicon is removed and the $70\text{-}\mu\text{m}$ -thick region has been reduced to a thickness of $50 \mu\text{m}$. The remaining poly is that which

remains in the grooves. An SiO_2 layer is then grown on the surface, and the wafers are ready for device processing.

In a report comparing the various SOI approaches, it was stated that bonded-wafer technologies exhibit very low leakage currents.⁸⁴ On the other hand, they are limited by the minimum thickness that can be achieved in the silicon and the minimum variation of that thickness across the wafer. This characteristic might still make SOI-by-wafer-bonding an attractive choice for advanced bipolar applications, as these require somewhat thicker silicon-device regions. In addition, it could be useful in some CMOS applications, such as those used for very low-power or high-voltage circuits, in which film thickness is not required to be minimized. A 1-kbit ECL SRAM fabricated on a bonded SOI wafer is described in reference 85.

A recently reported problem associated with the wafer-bonding process is that voids can occur at the interface between the wafers if a particle exists on the surface of either wafer (Fig. 2-53b). Such particles can keep two mechanically rigid surfaces from mating and bonding in the vicinity of the particle. The acute susceptibility of this bonding process to particles is reported to cause low production yield.¹²⁰

2.10.3 Silicon-on-Sapphire (SOS)

Another early SOI technology, begun in the 1960s, uses sapphire for both substrate and insulator (hence the name *silicon-on-sapphire*, or SOS). Sapphire has the advantage of being fairly well lattice-matched to silicon. Although there have been notable successes with SOS over the years, technology and material issues have prevented it from becoming a mainstream circuit technology. Recent advances in SOS, however, continue to preserve the viability of this material, and in the late 1980s it remained the only commercial, non-DI, SOI technology.⁸⁶ (More information about SOS can also be found in Vol. 1, chap. 5.)

2.10.4 Separation by Implanted Oxygen (SIMOX)

The creation of a buried layer of SiO_2 by implanting oxygen into silicon, a process known as SIMOX (for *separation by implanted oxygen*), is one of the major contenders for creating SOI structures.⁸⁷ The technique requires a high dose ($\sim 2 \times 10^{18} \text{ cm}^{-2}$) of oxygen (O^+) ions, as this provides the minimum concentration necessary to ensure that a continuous layer of stoichiometric SiO_2 will be formed by reaction of the oxygen with the silicon during the annealing process (Fig. 2-54).⁸⁸ The energy of the implant must also be high enough (150-180 keV) so that the peak of the implant is sufficiently deep within the silicon (0.3-0.5 μm). The wafer is normally heated to more than 400°C during the implantation process to ensure that the surface maintains its crystallinity during the high-dose implantation step (see Vol. 1, chap. 9 for more details on this topic).

A post-implant anneal is performed in a neutral ambient (N_2) for a sufficient time (3-5 hours) and at a high enough temperature (1100-1175°C) to form a buried layer of

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